W-CDMA SiGe TX-IC with high dynamic range and high power control accuracy

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Abstract — **This paper demonstrates the SiGe TX-IC for W-CDMA mobile terminals. For the TX-IC, a novel architecture of a variable gain amplifier is proposed to improve dynamic range and power control accuracy. With the 0.5 μm SiGe BiCMOS technology, this TX-IC achieved over 100 dB dynamic ranges within ±1.5dB accuracy over all temperatures. Output power of 7 dBm can be achieved by employment of P-MOSFET current mirror type self bias control circuit for the driver amplifier. Measurement results also satisfy the specification defined by 3GPP.**

I. Introduction

The popularization of the cellular phone brought higher demand of the small size, highly efficient terminal in the market. Recently, it is becoming a tendency to enjoy not only Internet access and e-mail, but also down loading the music and visual information. The W-CDMA system is expected to its high transmission rate for multimedia usage. The market requires a larger display and applications of higher layer. However, by the limitation of the terminal size and a battery capacity, the miniaturization and low current consumption of each component are always necessary. For the TX-IC that consists of transmitter functionalities except a HPA, low current consumptions and small sized implementation are needed. Also the W-CDMA system requires high dynamic range and high accuracy of power control, as well as low noise emission and low distortion for high capacity of communication traffics. These requirements of the W-CDMA system are defined in 3GPP [1]. For such requirements in W-CDMA TX-ICs, BiCMOS IF-IC [2] and GaAs RF-IC [3] are presented.

In this paper, the W-CDMA SiGe TX-IC is described. This TX-IC is implemented with the use of SiGe BiCMOS for the first fully integration of I/Q MOD, IF-VGA, UP-MIX, RF-VGA and Driver Amp. And the novel VGA architecture is proposed for improvement of dynamic range and control accuracy. In following discussions on IF-VGA circuit schematic and its behavior are described. Further more, experimental investigations are described for conformation of 3GPP specifications.

II. Architecture and Circuit Design

A. Architecture

In general, the W-CDMA transmitter consists of Antenna, RF Switch, Duplexer, Isolator, HPA, RF SAW, and TX-ICs. Base band differential input signals (I, Q) are provided from base band IC, RF and IF Carrier are provided from PLL Synthesizers.

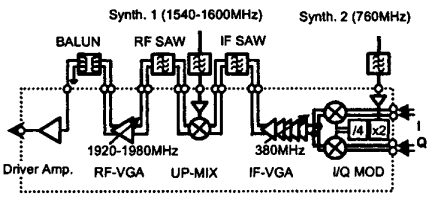

Fig. 1. Architecture of W-CDMA SiGe TXIC

Fig. 1 shows the Architecture of W-CDMA SiGe TXIC. It consists of balanced I-Q modulator (I/Q MOD), IF variable gain amplifier (IF-VGA), Up-converter (UP-MIX), RF variable gain amplifier (RF-VGA) and class A/B driver amplifier (Driver Amp). I/Q MOD and IF-VGA are connected internally on the silicon. IF–VGA and RF-VGA employ current constant architecture for constant IP1dB requirement. Off-chip IF and RF band pass filters are used to improve the out-of-band spurious and noise emission. Also an external balun converts differential port to single ended port.

For system level definition of the TX-IC, 95 dB of the power control is needed as a minimum requirement as below.

1) 74 dB for power control range defined by 3GPP
2) 12 dB for compensation of process variations
3) 9 dB for compensation of temperature variations

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For IF-VGA, a minimum 74 dB of gain control range is budgeted. And for RF-VGA, a minimum 21 dB of the gain control range, which is the summation of process compensation and temperature compensation, is budgeted.

B. I-Q Modulator (I/Q MOD)

The I/Q MOD employs a double balanced BiCMOS Gilbert cell mixer architecture. The base band I/Q inputs are fed into NFET differential pairs of the Gilbert cell. The single ended LO input signal is converted to a differential signal through an active balun and is multiplied for the quadrature phase generator.

C. *IF Variable Gain Amplifier (IF-VGA)*

The block diagram of IF-VGA is shown in Fig. 2. The IF-VGA includes five stage cascaded core amplifiers with linear gain control range more than 80 dB. Also five control circuits used for biasing offset control voltage of gain control for each core amplifier. And a BandGap circuit has an off-chip precision resistor for stabilization over processes.

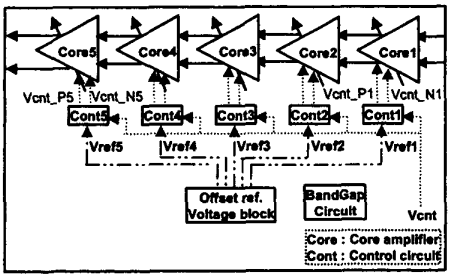

Fig. 2. The block diagram of IF-VGA

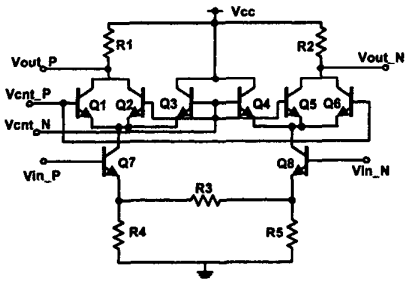

Fig. 3. The circuit schematic of core amplifier

Fig. 3 shows the circuit schematic of core amplifier. SiGe HBT's (Q1-Q6) are differential pairs, and they are driven by gain control voltage (Vcnt_P, Vcnt_N) to attenuate gain of the VGA. And the lower two SiGe HBT's (Q7, Q8) behave as a differential amplifier pair. SiGe HBT's (Q2, Q5) define the lower limit of the core amplifier gain range for the cascaded usage.

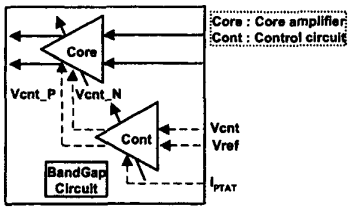

Fig. 4. The block diagram of core amplifier and control circuit

Fig. 4 shows the block diagram of core amplifier and control circuit. The Vref defines offset voltage for Vcnt_P and Vcnt_N. And the I_{PTAT} behaves as a control current to define the amplitude of Vcnt_P and Vcnt_N.

This IF-VGA has technical features as follows:

(a) Improvement of the control non-linearity by adding SiGe HBT's (Q2, Q5) in Fig. 3.
(b) Five stage core amplifiers topology for the improvement of the gain dynamic range.
(c) Compensation of gain error variation versus temperatures by the control circuit.

Firstly, the technical feature (a) is discussed. Fig. 5 shows the behavior of core amplifier gain curve. This VGA uses the technique of offset voltage allocations; each core amplifier has limitations for upper gain and lower gain. SiGe HBT's (Q1, Q6) in Fig. 3 define the upper gain limitation. And SiGe HBT's (Q2, Q5) in Fig. 3 define the lower gain limitation. The summation gain of previous stage and following stage, non-linear region of each core amplifiers are cancelled as shown in Fig.6. The summation gain is maintained linearly.

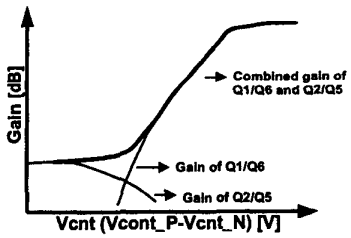

Fig. 5. The behavior of core amplifier gain curve

Next, the technical feature (b) is discussed. The behavior of the cascaded core amplifier is shown in Fig. 6. Each core amplifier has at least 20 dB gain control range and 16 dB accurate linear ranges. For the linear power control, gain range of each core amplifier is in offset allocation. For the offset behavior, the control circuit combines control voltage Vcnt and an offset reference

voltage Vref for generating Vcnt_P and Vcnt_N. And these voltages Vcnt_P, Vcnt_N control the gain of the core amplifier.

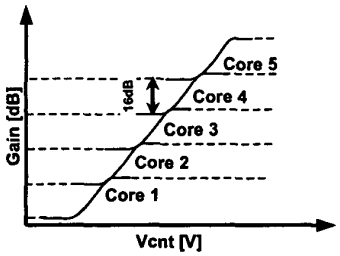

Fig. 6. The behavior of cascaded amplified gain curve.

Lastly, the technical feature (c) is discussed. Usually, the slope of the gain curve is changed due to the temperature changes. To maintain the slope (dB/V) over temperatures, the control circuit changes the amplitude of the gain control voltage by employing I_{PTAT} as shown in Fig.4. The behavior of control circuit over temperatures is also shown in Fig. 7.

Output P1dB of +1.5 dBm with total current consumption of 25 mA is achieved by employing an off-chip high Q, LC filter to the open collector output.

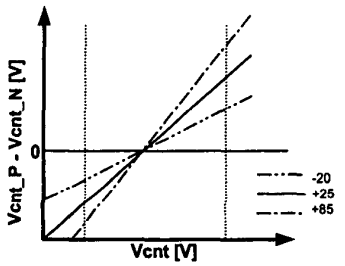

Fig. 7. The behavior of control circuit over temperatures

D. RF Up-Converter (UP-MIX)

The UP-MIX is a balanced Gilbert style mixer with a resistive feedback between Collector and Base in the lower differential pair to achieve the desired gain, and IP3. The upper quad HBT's behave as switching to improve NF. The mixer core and LO buffer are precisely biased by an on-chip BandGap circuit and off-chip precision resistor to tailor the bias current to achieve an optimum overall performance.

E. RF Variable Gain Amplifier (RF-VGA)

RF-VGA employs the same architecture as IF-VGA. The difference between IF-VGA and RF-VGA is operation range of gain curve, which directly affects the output power. To minimize the current consumption of RF-VGA, this VGA uses upper nonlinear region of its gain curve. And the use of nonlinear region helps expansion of control dynamic range.

This RF-VGA offers 30 dB gain control range and 18 dB of gain. It consumes 28 mA while providing +7 dBm of OP1dB and 5 dB of NF. Open collectors of the RF-VGA allow off-chip matching flexibility to improve linearity, gain for differential operation. An off-chip RF balun is used to convert balanced outputs to unbalanced signal. This off-chip flexibility helps in controlling cascaded performance in optimizing the first iteration of integrated design.

F. Class A/B Driver (Driver Amp)

Driver Amp is a single ended single-stage common emitter amplifier with C-B negative feedback for improved stability and linearity. The class AB design was chosen to achieve high linearity and low noise for minimum bias current of 16 mA. And the P-MOSFET current mirror type self-bias control circuit for biasing [4] is used to achieve very high linearity for low quiescent current consumption. The driver provides 14 dB gain, 4 dB of NF, and +12 dBm of OP1dB while consuming only 16mA of quiescent current. This amplifier has less than ± 2 dB variations over process and ±1 dB variations over temperatures and over supply voltages.

III. Experimental Results

A TX-IC for W-CDMA mobile terminals was implemented using 0.5 μm SiGe BiCMOS production technology. A photomicrograph of the chip is shown in Fig. 8. The active area of the IC is 2.54 mm × 2.54 mm and is compatible to be packaged in a 32 pin, exposed paddle BCC32++.

The cascaded Power Control Characteristic of the I/Q modulator and IF-VGA (IF Chain) over temperatures at IF-VGA Output are shown in Fig. 9. From –88 dBm to –6 dBm power control is confirmed by this measurement results. And gain error of linearity versus control voltage (0.26 V < Vcnt <2.54 V) with in ±1.5 dB is confirmed.

Another feature characteristic of this VGA is temperature characteristic. The gain error variation from room temperature is also shown in Fig. 10. This measurement results is confirmed that Gain control curve slides parallel to the curve of room temperature within ±1.5 dB over all control range.

For RF chain, the gain control range of -2 dB to 33 dB is also confirmed by the measurement. Measurements on individual building blocks and fully cascaded TX chains

are performed, and results are shown in Table I. The total current consumption of the TX-IC is approximately 97 mA, and it varies with power control level.

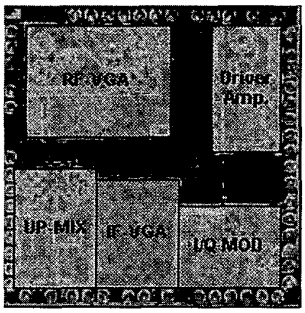

Fig. 8 Photomicrograph of TX-IC chip

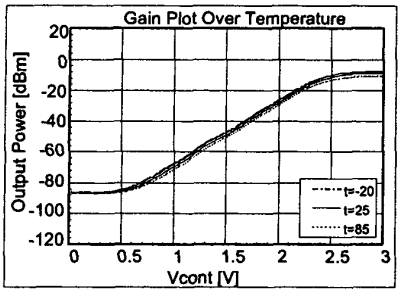

Fig. 9. The power control characteristic of IF Chain

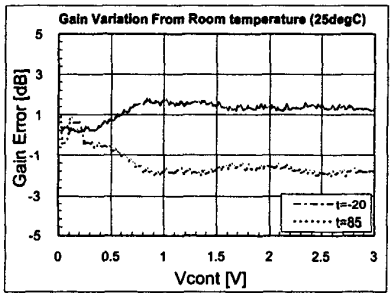

Fig. 10. The gain variation characteristic of IF Chain

TABLE I
SUMMARY OF TYPOGRAPHICAL SETTINGS

Maximum CH Power	7.0 dBm	@1950MHz
Minimum CH Power	-82.8 dBm	@1950MHz
Power Control Range	89.9 dB	@1950MHz
OBW	4.2 MHz	@+7dBm output
ACLR	-47.6 dBc	@+5MHz
	-48.1 dBc	@-5MHz
	-68.2 dBc	@+10MHz
	-69.9 dBc	@-10MHz
EVM	6.3 %rms	@+7dBm output

IV. CONCLUSION

SiGe TX-IC for W-CDMA mobile terminals with the novel architecture of a variable gain amplifier is proposed for improvement of dynamic range and power control accuracy. With 0.5 μm SiGe BiCMOS technology, this TX-IC achieved over 100 dB (IF-VGA: 82 dB, RF-VGA: 35dB) dynamic ranges within ±1.5 dB accuracy over all temperatures.

The maximum output modulated power of +7 dBm, -46 dBc ACLR at 5 MHz offset, and RMS EVM of 6.3 % are achieved by employment of P-MOSFET current mirror type self bias control circuit for a driver amplifier.

Measurement results also satisfy the specification defined by 3GPP. It consumes 290 mW of total power for 3.0 V typical voltage supply.

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